What Is Claimed Is:

1. An array substrate for a liquid crystal display device, comprising:

a gate line;

a data line including a first data line having a first width and a second data line having a second width overlying the first data line, the second width is larger than the first width;

a pixel electrode in a pixel region and defined by a crossing of the gate line and the data line, the pixel electrode being formed during a same process as the second data line; and

a thin film transistor connected to the pixel electrode.

2. The device according to claim 1, further includes an insulating layer between the first data line and the second data line, and at least one data contact hole in each pixel region for connecting the first data line and the second data line.

3. The device according to claim 2, further includes a passivation layer between the first data line and the second data line on the thin film transistor.

4. The device according to claim 3, wherein the passivation layer and the insulating layer are simultaneously formed during a same process.

5. The device according to claim 1, wherein the first data line includes at least one of molybdenum (Mo), tungsten (W), chromium (Cr), and nickel (Ni).

6. The device according to claim 1, wherein the second data line and the pixel electrode include at least a transparent conductive material.

7. The device according to claim 6, wherein the transparent conductive material includes at least indium tin oxide (ITO).

8. The device according to claim 1, wherein the thin film transistor includes the gate electrode, a first source electrode having a first width connected to the first data line, a second source electrode having a second width connected to the second data line, and a drain electrode spaced apart from the first source electrode.

9. The device according to claim 8, wherein the second source electrode is formed over the first source electrode.

10. The device according to claim 9, wherein the second width of the second source electrode is larger than the first width of the first source electrode.

11. A manufacturing method of an array substrate for a liquid crystal display device, comprising:

forming a gate line on a transparent substrate, the gate line includes a gate electrode;

forming a gate insulating layer and a semiconductor layer over the gate line;

forming a first data line having a first width and a drain electrode on the gate insulating layer and on the semiconductor layer, the first data line includes a first source electrode that crosses the gate line;

forming a passivation layer on the first source electrode, the first data line and the drain electrode, the passivation layer includes a drain contact hole and a data contact hole; and

forming a pixel electrode, a second data line having a second width and a second source electrode, the pixel electrode connected to the drain electrode through the drain contact hole, and the second data line connected to the first data line and the first source electrode through the data contact hole.

12. The method according to claim 11, wherein the array substrate is formed using a photolithographic masking process, and the pixel electrode, the second data line and the second source electrode are simultaneously patterned during a same light exposure process.

13. The method according to claim 11, wherein the second width of the second data line is larger than the first width of the first data line.

14. The method according to claim 9, wherein the pixel electrode, the second data line and the second source electrode include at least a transparent conductive material.

15. The method according to claim 14, wherein the transparent conductive material includes indium tin oxide (ITO).

16. The method according to claim 10, wherein the drain electrode, the first data line and the first source electrode include at least one of molybdenum (Mo), tungsten (W), chromium (Cr), and nickel (Ni).

17. A manufacturing method of an array substrate for a liquid crystal display device, comprising:

forming a gate line;

forming a data line including a first data line having a first width and a second data line having a second width larger than the first width;

forming a pixel electrode in a pixel region defined by a crossing of the gate line and the data line; and

forming a thin film transistor connected to the pixel electrode.

18. The method according to claim 17, wherein the pixel electrode and the second data line are simultaneously formed during a same process.

19. The method according to claim 17, further includes forming an insulating layer between the first data line and the second data line

20. The method according to claim 19, further includes forming at least one data contact hole in each pixel region for connecting the first data line and the second data line.

21. The method according to claim 19, further includes forming a passivation layer between the first data and the second data line on the thin film transistor.

22. The method according to claim 21, wherein the passivation layer and the insulating layer are simultaneously formed during a same process.

23. The method according to claim 17, wherein the first data line includes at least one of molybdenum (Mo), tungsten (W), chromium (Cr), and nickel (Ni).

24. The method according to claim 17, wherein the second data line and the pixel electrode include at least a transparent conductive material.

25. The method according to claim 24, wherein the transparent conductive material includes at least indium tin oxide (ITO).

26. The method according to claim 17, wherein forming the thin film transistor includes forming a first source electrode having a first width connected to the first data line, forming a second source electrode having a second width connected to the second data line, and forming a drain electrode spaced apart from the first source electrode.

27. The method according to claim 26, wherein the second source electrode is formed over the first source electrode.

28. The method according to claim 27, wherein the second width of the second source electrode is larger than the first width of the first source electrode.